# LAMPIRAN

- 1. ATMEGA 8
- 2. TSOP 1738
- 3. IRF 540N

### atures

gh-performance, Low-power Atmel®AVR® 8-bit Microcontroller Ivanced RISC Architecture

- 130 Powerful Instructions - Most Single-clock Cycle Execution

32 x 8 General Purpose Working Registers

- Fully Static Operation

- Up to 16MIPS Throughput at 16MHz

On-chip 2-cycle Multiplier

h Endurance Non-volatile Memory segments

8Kbytes of In-System Self-programmable Flash program memory

- 512Bytes EEPROM

- 1Kbyte Internal SRAM

- Write/Erase Cycles: 10,000 Flash/100,000 EEPROM

Data retention: 20 years at 85°C/100 years at 25°C(1)

Optional Boot Code Section with Independent Lock Bits

In-System Programming by On-chip Boot Program

True Read-While-Write Operation

Programming Lock for Software Security

ripheral Features

Two 8-bit Timer/Counters with Separate Prescaler, one Compare Mode

One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture

Mode

Real Time Counter with Separate Oscillator

Three PWM Channels

8-channel ADC in TQFP and QFN/MLF package

Eight Channels 10-bit Accuracy

6-channel ADC in PDIP package

Six Channels 10-bit Accuracy

Byte-oriented Two-wire Serial Interface

Programmable Serial USART

Master/Slave SPI Serial Interface

Programmable Watchdog Timer with Separate On-chip Oscillator

On-chip Analog Comparator

ecial Microcontroller Features

Power-on Reset and Programmable Brown-out Detection

Internal Calibrated RC Oscillator

External and Internal Interrupt Sources

Five Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, and

Standby

and Packages

23 Programmable VO Lines

28-lead PDIP, 32-lead TQFP, and 32-pad QFN/MLF

erating Voltages

2.7V - 5.5V (ATmega8L)

4.5V - 5.5V (ATmega8)

ed Grades

0 - 8MHz (ATmega8L)

0 - 16MHz (ATmega8)

ver Consumption at 4Mhz, 3V, 25°C

Active: 3.6mA

Idle Mode: 1.0mA

Power-down Mode: 0.5µA

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8-bit Atmel with 8KBytes In-System Programmable Flash

ATmega8 ATmega8L

Summary

Rev.2486AAS-AVR-02/2013

# PDIP nfigurations (RESET) PC6 [ 1 (RXD) PD0 [ 2 (TXD) PD1 [ 3 28 PC5 (ADC5/SCL) 27 PC4 (ADC4/SDA) 26 PC3 (ADC3) 25 PC2 (ADC2) 24 PC1 (ADC1) (INTO) PD2 4 (INT1) PD3 C 5 23 PC0 (ADC0) 22 GND 21 JAREF (XCK/T0) PD4 ☐ 6 VCC 7 GND 20 AVCC 19 PB5 (SCK) (XTAL1/TOSC1) PB6 29 (XTAL2/TOSC1) PBS [ 9] (XTAL2/TOSC2) PB7 [ 10 (T1) PD5 [ 11 (AIN0) PD5 [ 12 (AIN1) PD7 [ 13 (ICP1) PB0 [ 14 18 PB4 (MISO) 17 PB3 (MOSI/OC2) 16 PB2 (SS/OC1B) 15 PB1 (OC1A) **TQFP Top View** 1 PD2 (INT0) 1 PD1 (TXD) 1 PD0 (RXD) 1 PC3 (RESET) 1 PC3 (ADGS/SCL) 1 PC4 (ADGA/SDA) 1 PC3 (ADG3) 22888888 24 PC1 (ADC1) 23 PC0 (ADC0) 22 DADC7 21 DGND (INT1) PD3 [ 1 (XCK/T0) PD4 [ GND D vcc | 20 AREF 19 ADC6 18 AVCC 17 PB5 (SCK) GND VCC [ 6 (XTALI/TOSCI) PB6 7 (XTAL2/TOSC2) PB7 6 (AIN) PDS (1) PDS **MLF Top View** 22 | PD2 (INTO) 31 | PD1 (TXD) 30 | PD0 (RXD) 29 | PC6 (RESET) 28 | PC6 (RESET) 27 | PC4 (ADC4/SD1) 26 | PC3 (ADC3) 25 | PC2 (ADC3) O (INT1) PD3 24 PC1 (ADC1) (XCK/TO) PD4 23 PC0 (ADC0) 22 | ADC7 21 | GND 20 | AREF GNDC3 VCCE GND 5 VCCE 19 ADC6 (XTAL1/TOSC1) PB6 AVCC 17 PB5 (SCK) (XTAL2/TOSC2) PB7 (AIN) PDS (10 (AIN) PDS (10 (AIN) PDS (10 (AIN) PDS (11 (AIN) PDS (12 (AIN) PB (13 (AINS) PB (AI NOTE: The large center pad undermosth the MLF packages is made of metal and internally connected to GND. It would be soldered or glued to the PGB to ensure good mechanical slability. If the center good tell unconnected, the package might loosen from the PGB.

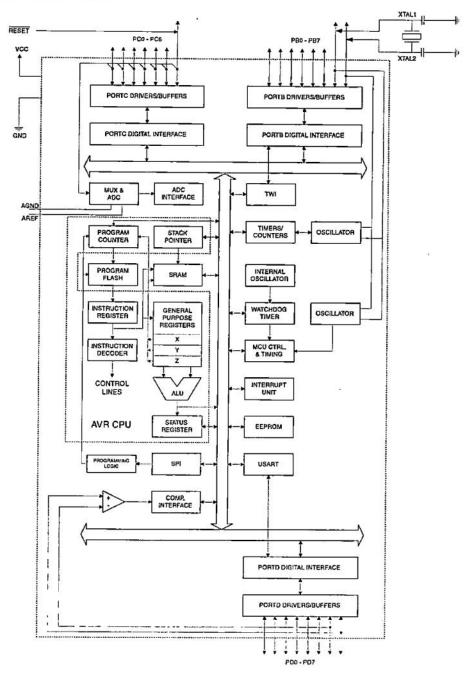
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erview

The Atmel®AVR® ATmega8 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega8 achieves throughputs approaching 1MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed.

ck Diagram

Figure 1. Block Diagram



The Atmet AVR® core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega8 provides the following features: 8 Kbytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes of EEPROM, 1 Kbyte of SRAM, 23 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, a 6-channel ADC (eight channels in TQFP and QFN/MLF packages) with 10-bit accuracy, a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next Interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The Flash Program memory can be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash Section will continue to run while the Application Flash Section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega8 is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many embedded control applications.

The ATmega8 is supported with a full suite of program and system development tools, including C compilers, macro assemblers, program simulators, and evaluation kits.

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Minimum and Maximum values will be available after the device is characterized.

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## Descriptions

Digital supply voltage.

Ground.

#### B (PB7..PB0) L1/XTAL2/TOSC1/ C2

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Depending on the clock selection fuse settings, PB6 can be used as input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

Depending on the clock selection fuse settings, PB7 can be used as output from the inverting Oscillator amplifier.

If the Internal Calibrated RC Oscillator is used as chip clock source, PB7..6 is used as TOSC2..1 input for the Asynchronous Timer/Counter2 if the AS2 bit in ASSR is set.

The various special features of Port B are elaborated in "Alternate Functions of Port B" on page 58 and "System Clock and Clock Options" on page 25.

#### C (PC5..PC0)

Port C is an 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

## RESET

If the RSTDISBL Fuse is programmed, PC6 is used as an I/O pin. Note that the electrical characteristics of PC6 differ from those of the other pins of Port C.

If the RSTDISBL Fuse is unprogrammed, PC6 is used as a Reset input. A low level on this pin for longer than the minimum pulse length will generate a Reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 38. Shorter pulses are not guaranteed to generate a Reset.

The various special features of Port C are elaborated on page 61.

#### D (PD7..PD0)

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Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega8 as listed on page 63.

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 38. Shorter pulses are not guaranteed to generate a reset.

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# lering Information

peėd (MHz)	Power Supply (V)	Ordering Code <sup>(2)</sup>	Package <sup>(1)</sup>	Operation Range	
8	2.7 - 5.5	ATmega8L-8AU ATmega8L-8AUR <sup>(3)</sup> ATmega8L-8PU ATmega8L-8MU ATmega8L-8MUR <sup>(3)</sup>	32A 32A 28P3 32M1-A 32M1-A	Industrial	
16	4.5 - 5.5	ATmega8-16AU ATmega8-16AUR <sup>(3)</sup> ATmega8-16PU ATmega8-16MU ATmega8-16MUR <sup>(3)</sup>	32A 32A 28P3 32M1-A 32M1-A	(-40°C to 85°C)	
8	2.7 - 5.5	ATmega8L-8AN ATmega8L-8ANR <sup>(3)</sup> ATmega8L-8PN ATmega8L-8MN ATmega8L-8MUR <sup>(3)</sup>	32A 32A 28P3 32M1-A 32M1-A	Industrial (-40°C to 105°C)	
16	4.5 - 5.5	ATmega8-16AN ATmega8-16ANR <sup>(3)</sup> ATmega8-16PN ATmega8-16MN ATmega8-16MUR <sup>(3)</sup>	32A 32A 28P3 32M1-A 32M1-A		

This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities

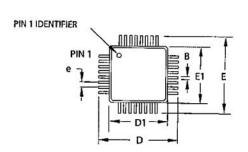
	Package Type
	32-lead, Thin (1.0mm) Plastic Quad Flat Package (TQFP)
	28-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
1-A	32-pad, 5 x 5 x 1.0 body, Lead Pitch 0.50mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green

<sup>3.</sup> Tape & Reel

<sup>4.</sup> See characterization specification at 105°C

# ckaging Information





#### COMMON DIMENSIONS (Unit of measure = mm)

			20596	
SYMBOL	MIN	NOM	MAX	NOTE
Α	-	N=	1.20	
A1	0.05	-	0.15	
A2	0.95	1.00	1.05	_
D	8.75	9.00	9.25	
D1	6,90	7.00	7.10	Note 2
E	8,75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
В	0.30	-	0.45	
c	0.09		0.20	
L	0.45	-	0.75	
e		0.80 TYP		

# 2010-10-20

. This package conforms to JEDEC reference MS-026, Variat	ion ABA.
2. Dimensions D1 and E1 do not include mold protrusion.	Allowable
protrusion is 0.25mm per side. Dimensions D1 and E1 are	maximum
plastic body size dimensions including mold mismatch.	
3. Lead coplanarity is 0.10mm maximum.	

TITLE

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32A, 32-lead, 7 x 7mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)

DRAWING NO. REV. 32A C

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